Contact: Prof. Weidong Zhou

UTA-1: Devices and architectures for high-dimensional entanglement

(Area 4: Quantum computing/communications/information)

PI: Prof. Michael Vasilyev, Photonics Center and Department of EE, UT Arlington

DESCRIPTION: We will develop photonic devices and architectures for generation, distribution, and manipulation / processing of high-dimensional entangled states for applications in quantum computing, communication, and sensing. This work builds upon our existing research on using polarization, frequency / temporal, and spatial modes to scale quantum communication and processing capacity, supported by the Quantum Testbed at the UT Arlington.

UTA-2: Photonic crystal optoelectronics for quantum photonics

(Area 5: Quantum & Nanophotonics)

PI: Prof. Weidong Zhou, Photonics Center and Department of EE, UT Arlington

DESCRIPTION: We are developing high power semiconductor photonic crystal surface emitting lasers (PCSELs) and high-speed photonic crystal spatial light modulators (PCSLMs) for integrated quantum photonic chips. These are currently funded by US Department of Defense. We hope to establish collaborations in materials, designs, and heterogeneous integration with our counterparts in Taiwan.

UTA-3: Advancing 1.55 µm Single-Photon Detectors for Quantum Technology

(Area 5: Quantum & Nanophotonics)

PI: Prof. Seunghyun (Jacob) Lee, Photonics Center and Department of EE, UT Arlington

DESCRIPTION: We are planning to develop highly sensitive photodetectors using avalanche photodiodes (APDs), designed for single-photon detectors. Our research focuses on an integrated design approach that combines electronic engineering with photonic engineering to create advanced APDs. The design, fabrication and characterization of the APDs will be performed using facilities at UT Arlington. We aim to establish collaborations in material development and heterogeneous integration with our counterparts in Taiwan.

Contact: Massimo Fischetti

UTD-1: Materials for Future VLSI

(Covered under the Anstrom Semiconductor Initiative)

PIs: Profs. KJ Cho, William Vandenberghe, Chadwin Young, Massimo Fischetti

DESCRIPTION: We propose to study new two-dimensional (2D) materials with possible applications to the scaling of electron devices for future technology nodes. Professor Cho is an expert *in ab initio* calculations (density functional theory, DFT) that can be used to study the structural, mechanical, electronic, optical, and magnetic properties of these materials (as well as their growth). Professors Vandenberghe and Massimo combine the use of such DFT calculations to study theoretically electronic transport in these materials and to simulate the performance and characteristics of field-effect transistors (FETs) below the 10 nm scale, together with the physics of the electrical contacts that must be made to these materials. Finally, professor Young is an expert in the electrical characterization and reliability of electron devices and adds an experimental aspect to the effort.

Contact: Eric Brey

UTSA-1: Light-speed LLM at Minimal Energy Cost with Next-generation Silicon Photonics

DESCRIPTION: The wide adoption and large-scale compute cost of Large Language Models (LLMs), e.g., Vision Trans- formers, have called for efficient hardware accelerators. While traditional CMOS accelerators are being commonly deployed , there is a rising trend of utilizing silicon photonics (SiPh) as a promising alternative owing to its ultralow power consumption and light-speed processing capability. There have been limited attempts at using SiPh for designing AI accelerators that operate with hardcoded weight matrices (e.g. CNN inference). However, such designs fail to perform LLM-like models due to their highly dynamic attention mechanism. In this collaborative effort, I plan to pursue a codesign approach going from photonic device modeling to full-scale photonic system optimization to realize next-generation all-photonic LLM accelerator specifically for time-critical and resource constraint scenarios such as healthcare and remote sensing.

UTSA-2: Improving Semiconductor Manufacturing through a Lean AI Paradigm: An AI-aided Lean and Smart System for Semiconductor Production Considering Green and Sustainable Measures

DESCRIPTION: Integrating Lean Manufacturing tools with artificial intelligence (AI) is emerging as a revolutionary approach to optimize production processes, reduce waste, and enhance efficiency. Traditional Lean practices focus on waste reduction and process improvement, often relying on human expertise for problem identification and resolution. AI algorithms, on the other hand, excel in pattern recognition, data analysis, and decision-making. Lean tools and AI can offer more precise, data-driven solutions for common manufacturing challenges when integrated. AI algorithms can automate and refine Lean techniques like value stream mapping, Kanban, and 5S by providing real-time, actionable insights drawn from big data. This fusion of Lean and AI aids in predictive maintenance, quality control, and optimization, enhancing the efficiency and responsiveness of the manufacturing process, and

addressing important green and sustainable measures. Moreover, AI’s capability for machine learning allows the system to adapt and improve autonomously over time, further aligning with Lean’s continuous improvement ethos.

UTAT-1: Physical design for advanced packaging

(Area 1: Advanced VLSI)

PI: Prof. David Z. Pan, Department of ECE, UT Austin

Prof. Shao-Yun Fang, EE, NTUST

DESCRIPTION: Physical design in advanced packaging and heterogeneous integration involves integrating multiple semiconductor devices into a single package to improve performance, power, and area (PPA). Key techniques include 3D integration for vertical stacking, 2.5D integration using interposers for high-density interconnects, and Fan-Out Wafer-Level Packaging (FOWLP) for compact designs. System-in-Package (SiP) and chiplet-based designs allow modular integration of diverse functionalities. Advanced interconnects, such as high-density interconnects (HDI) and micro-bumps, facilitate die-to-die connections. Embedded die packaging, advanced materials, and efficient thermal management improve electrical performance and reliability. These techniques enable the creation of powerful, efficient, and compact electronic systems, meeting the demands of modern applications.

UTAT-2: Heterogeneous integration and hardware/software co-design for AI acceleration

(Area 1: Advanced VLSI)

PI: Prof. Diana Marculescu (Department Chair), Department of ECE, UT Austin

Prof. Shao-Yun Fang, EE, NTUST

DESCRIPTION: To strengthen the need for 2.5D/3D integration of multiple semiconductor devices, specific applications such as computer vision (CV) and natural language processing (NLP) are widely discussed. These applications usually involve massive amount of data exchange between computing/memory units, necessitating high-speed communication that can be realized by 2.5D/3D integration. In addition to aforementioned intrinsic characteristics of CV and NLP applications, accelerating these applications may further uplift the communication requirement and thus make it imperative to develop advanced integration and packaging techniques. The synergy between advanced integration/packaging techniques and CV/NLP acceleration approaches is also a highly challenging topic to be addressed.

Contact: Prof. Hsiu-Yang Tseng (Department of Mechanical Engineering, NTUST)

Project Type: Research

Title: Advancing nanoscale wet etching efficacy in semiconductor fabrication

As semiconductor miniaturization pushes technological limits, refining manufacturing processes, such as wet etching, is crucial in the competition for higher yields and performance. In this project, we target the improvement of delivery of etchants and consequent removal of etching by products in nanoscale features. Focused on optimizing the hydrodynamic boundary layer at the liquid-solid interface by introducing electroosmotic flow pumping, this approach aims to enhance the precision of etching nanoscale features, contributing to more effective wafer processing and reliable semiconductor devices.

Project Type: Talent Cultivation/Exchange

Title: Academic activities and a short course for semiconductor manufacturing process, equipment, and measurement technology

We plan to open a short course introducing semiconductor equipment for manufacturing and measurement purposes, such as vacuum, thin film, plasma, photolithography, chemical mechanical polishing, electrical discharge machining, packaging, and precision measurement. Academic activities and exchange programs between UAAT and UTS will also be arranged.

Contact: Prof. Ming-Jyh Chern (Department of Mechanical Engineering, NTUST)